WHAT IS CLAIMED IS:

1. A method of testing at least one mixed signal semiconductor device, the method comprising:

executing a first test for the at least one mixed signal semiconductor device;

preparing execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

processing test data resulting from the first test; and

executing the second test concurrently with the processing of the test data.

2. A method according to claim 1, wherein the mixed signal semiconductor testing is performed by a single processor.

3. A method according to claim 2, wherein the executing the first test comprises:

configuring hardware elements corresponding to the first test in a mixed signal semiconductor device tester unit; and

executing one or more test scripts corresponding to the first test, wherein the one or more test scripts include at least one command executable on the processor and the mixed signal semiconductor device tester unit is coupled to the processor.

4. A method according to claim 1, wherein the preparing execution of the second test comprises:

identifying hardware elements corresponding to the second test; and

configuring the hardware elements corresponding to the second test.

5. A method according to claim 1, wherein the first and the second tests are configured for one or more of wafer testing and package testing of the mixed signal semiconductor device.

6. A method according to claim 1, wherein the first and second tests are configured in an interpreted software language.

7. A method according to claim 6, wherein the interpreted software language is Interactive Test Pascal.

8. A method according to claim 2, further comprising:

storing the test data resulting from the first test in a first information storage, wherein the first information storage is shared by a plurality of software computation modules concurrently executing on the processor.

9. A method according to claim 8, wherein the plurality of software computation modules are configured in at least one compiled software language.

10. A method according to claim 8, further comprising:

storing results of the processing of the test data in a second information storage, wherein the second information storage is shared by the plurality of software computation modules.

11. A method according to claim 10, wherein the first and second information storage are configured in a single storage unit.

12. An apparatus for testing at least one mixed signal semiconductor device comprising:

at least one processor; and

at least one device tester unit coupled to the processor, wherein the processor is configured to

execute a first test for the at least one mixed signal semiconductor device;

prepare execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

process test data resulting from the first test; and

execute the second test concurrently with the processing of the test data.

13. An apparatus according to claim 12, wherein the device tester unit comprises a plurality of hardware modules for testing the at least one mixed signal semiconductor device.

14. An apparatus according to claim 12, further comprising:

at least one device interface unit coupled to the at least one processor and configured to provide signal interface for the at least one mixed signal semiconductor device.

15. An apparatus according to claim 12, wherein the mixed signal semiconductor testing is performed by a single processor.

16. An apparatus according to claim 15, wherein the processor is further configured to

configure hardware elements corresponding to the first test in a mixed signal semiconductor device tester unit; and

execute one or more test scripts corresponding to the first test, wherein the one or more test scripts include at least one command executable on the processor and the mixed signal semiconductor device tester unit is coupled to the processor.

17. An apparatus according to claim 15, wherein the processor is further configured to

identify hardware elements corresponding to the second test; and

configure the hardware elements corresponding to the second test.

18. An apparatus according to claim 15, wherein the first and the second tests are configured for one or more of wafer testing and package testing of the mixed signal semiconductor device.

19. An apparatus according to claim 15, wherein the first and second tests are configured in an interpreted software language.

20. An apparatus according to claim 15, wherein the interpreted software language is Interactive Test Pascal.

21. An apparatus according to claim 15, further comprising:

a first information storage coupled to the processor, wherein the processor is further configured to

store the test data resulting from the first test in the first information storage, wherein the first information storage is shared by a plurality of software computation modules concurrently executing on the processor.

22. An apparatus according to claim 21, wherein the plurality of software computation modules are configured in at least one compiled software language.

23. An apparatus according to claim 21, further comprising:

a second information storage coupled to the processor, wherein the processor is further configured to

store results of the processing of the test data in a second information storage, wherein the second information storage is shared by the plurality of software computation modules.

24. An apparatus according to claim 23, wherein the first and second information storage are configured in a single storage unit.

25. A computer program product comprising a set of instructions configured to enable a mixed signal semiconductor device test system to

execute a first test for at least one mixed signal semiconductor device;

prepare execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

process test data resulting from the first test; and

execute the second test concurrently with the processing of the test data.

26. A computer program product according to claim 25, wherein the set of instructions are executed on a single processor.

27. A computer program product according to claim 26, wherein the set of instructions are further configured to

configure hardware elements corresponding to the first test in a mixed signal semiconductor device tester unit; and

execute one or more test scripts corresponding to the first test, wherein the one or more test scripts include at least one command executable on the processor and the mixed signal semiconductor device tester unit is coupled to the processor.

28. A computer program product according to claim 26, wherein the set of instructions are further configured to

identify hardware elements corresponding to the second test; and

configure the hardware elements corresponding to the second test.

29. A computer program product according to claim 26, wherein the first and the second tests are configured for one or more of wafer testing and package testing of the mixed signal semiconductor device.

30. A computer program product according to claim 26, wherein the set of instructions are configured in an interpreted software language.

31. A computer program product according to claim 30, wherein the interpreted software language is Interactive Test Pascal.

32. A computer program product according to claim 26, wherein the set of instructions are further configured to

store the test data resulting from the first test in a first information storage, wherein the first information storage is shared by a plurality of software computation modules concurrently executing on the processor.

33. A computer program product according to claim 32, wherein the plurality of software computation modules are configured in at least one compiled software language.

34. A computer program product according to claim 32, wherein the set of instructions are further configured to

store results of the processing of the test data in a second information storage, wherein the second information storage is shared by the plurality of software computation modules.